CLAIM

13.A wafer level package for producing chip size packages, comprising:

a plurality of chips on a surface of a wafer having trenches running through, each said trench formed between said chips;

a filling material filled in said trenches;

metal pads formed on the surface of said wafer;

a photosensitive polymer layer formed on the surface of said wafer and exposing said metal pads;

a first conductive layer formed on said metal pads within said photosensitive polymer layer;

a circuit distribution pattern formed on the top of said photosensitive polymer layer and said first conductive layer;

a protection layer covered on said circuit distribution pattern, said photosensitive polymer layer and a portion of said circuit distribution pattern exposed; and

conductive bumps formed on said exposed circuit distribution pattern.

14. The wafer level package for producing chip size packages according to claim 13, wherein said photosensitive polymer layer comprises epoxy.

15. The wafer level package for producing chip size packages according to claim 13, wherein said photosensitive polymer layer comprises photosensitive polyimide.

16. The wafer level package for producing chip size packages according to claim 13, wherein said filling material comprises epoxy.

17. The wafer level package for producing chip size packages according to claim 13, wherein said protection layer comprises epoxy.

18. The wafer level package for producing chip size packages according to claim 13, wherein said circuit distribution pattern comprises copper.

19. The wafer level package for producing chip size packages according to claim 13, wherein said conductive bump comprises solders